Where is the Packaging Technology Drifting? : Speed/Flexibility

Choon Lee l COO and CTO
Agenda

- Technology trend
- Amkor packaging solution
- New society proposal
Vacuum tube

Transistor invention _ 1949 year

IC invention _ 1958 year

VLSI introduction _ 1970s

ENIAC (Electronic Numerical Integrator And Computer) _ 1946

IBM System 360 _ 1964

TRADIAC (TRAnistor DIgital Computer) _ 1955

Apple II _ 1977
Computing trend

- **Mainframe Computing Era**
- **Personal Computing Era**
- **Mobile Computing Era**
- **Internet of Things Era**

Year:
- 1950
- 1980
- 2010
- 2020

Market:
New growth driver

Price War

With IoT

Competing hardware specs

H/W innovation

자료: HMC투자증권.
Electronics in Everything – The Light Bulb

- For 70+ years the common light bulb contained no electronics.
- Then in the 1970’s, CFL bulbs included a small power converter.
- Today the LED bulb contains a power supply, driver circuits, dimmers, etc.
- Soon bulbs will contain WiFi or Bluetooth radios and microcontrollers for remote operation.
X-ray Image of the L-Prize Winning LED Lamp

Philips Lighting
Q) What’s the packaging solution for IoT era?

Electronics in Everything

IOT

Things  Transmission  Gateway  Big data  Decision
A) The answer is Miniaturization and Integration!
Q) What’s the technology solution for new development paradigm?

Yesterday
- Time Interval
- Debugging Time
- Formalized

Today
- No Time Interval
- No Debugging Time
- Flexible
A) The answer is wide packaging experience and process readiness!
Amkor Packaging Experience

1980 era

1990 era

2000 era

2010 era

PDIP
Metal can
CERDIP
PBGA
Super BGA
fBGA
CABGA
TABGA
tfpCSP
Plated Bump
Vision Pak
SIP
MLF
Stacked CSP
Memory Card
Past Bump
Camera Module
PoP
FlipStack® CSP
Fusion Quad®
Thru Mold Via PoP
FC®BGA
MEMS microphone
Cu Pillar Bump
tfpCSP
2.5/3D Stacks, TSV
WLFO
POSSUM™
Amkor One-stop and Total Solution

Design

Simulation

Development

Production

Testing

Analysis
Leadframe Package Innovation

- Even matured leadframe package, the innovation named routable is achieved.

MQFP  TQFP  MLF  RtMLF

Smaller  Thinner  Routable
RtMLF ( Routable MLF )

- **What is RtMLF?**
  - Resin filled trace available 1L substrate (MLF)
  - Low cost and small form factor driven structure
  - For server, PC, game console as well as mobile peripheral

- **Interconnection method**
  - Wire Bonding, Flip Chip

- **Development status**
  - Body size: ~10x10mm
  - I/O count: ~176
WLCSP is moving

- Mid I/O packages are converted to WLCSP due to form factor/cost

Finer pitch: More I/O, smaller chip

BLR performance: Large die solution

Thinner WLCSP

12 x 12 rtCSP = 400 I/O

44%

8 x 8 WLCSP = 400 I/O
WLCSP Large Die Solution

- WLCSP with mold structure is to improve solder joint performance

<table>
<thead>
<tr>
<th>BD size. (mm)</th>
<th>Die thick (um)</th>
<th>Ball size (um)</th>
<th>Ball Alloy</th>
<th>TC 1st fail</th>
<th>Mean life</th>
<th>TC 1st fail</th>
<th>Mean life</th>
</tr>
</thead>
<tbody>
<tr>
<td>10x10</td>
<td>350</td>
<td>250</td>
<td>SACQ</td>
<td>1225</td>
<td>2849</td>
<td>179</td>
<td>1228*</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>SB05</td>
<td>836</td>
<td>1944</td>
<td>251</td>
<td>1442*</td>
</tr>
</tbody>
</table>

* Mean life is extrapolated because failure ratio is less than 50%
New Concept Technology without TSV

- Higher Performance
- Integration
- Cost benefit

**SLIM™**

Silicon-Less Integrated Module

**SWIFT™**

Silicon Wafer Integrated Fan-out Technology

- **Top die**
- **U-bump solder joint**
- **Fab. BEOL layer**
- **RDL layer**
- **BGA**
SWIFT covers Flip Chip CSP and SiP application

Molded 12inch CoW wafer processing
- Available

Fine L/S multi RDL
- 5/5um available
- 3L RDL demonstrated

Backside pattern reveal and carrier attach
- Available

Tall Cu pillar for memory interface
- 180um tall Cu demonstrated

Fine pitch u-bump interconnection
- CoW chip attach with mass reflow
- 40/45um available
- 30um demonstrated

Integration
Logic and Memory package stack

**Body size**
- 8~17mm

**Mold**
- MUF
- Exposed die
- Bare die
- Strip grinding

**BGA ball pitch**
- 0.35mm/0.30mm

**DAF**
- 5um thick

**Thin die**
- 20um thick

**High memory I/O**
- Fan-in PoP
- Fine pitch TMV (~0.2mm)

**Interconnection**
- Solder bump
- Cu pillar

**Chip attach**
- LAB
- TCNCP
- MR

**Substrate**
- ETS
- Coreless
# Thin PoP Roadmap

<table>
<thead>
<tr>
<th></th>
<th>Available</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
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<tbody>
<tr>
<td>Memory thickness</td>
<td>0.43</td>
<td>0.39</td>
<td>0.36</td>
<td>0.35</td>
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<tr>
<td></td>
<td>(assumption)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exposed die TMV</td>
<td>0.69</td>
<td>0.60</td>
<td>0.51</td>
<td>0.48</td>
</tr>
<tr>
<td></td>
<td>1.12</td>
<td>0.99</td>
<td>0.87</td>
<td>0.83</td>
</tr>
<tr>
<td></td>
<td>(max thickness)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bare die TMV</td>
<td>0.69</td>
<td>0.65</td>
<td>0.63</td>
<td>0.62</td>
</tr>
<tr>
<td></td>
<td>1.12</td>
<td>1.04</td>
<td>0.99</td>
<td>0.97</td>
</tr>
<tr>
<td>Interposer TMV</td>
<td>0.71</td>
<td>0.65</td>
<td>0.61</td>
<td>0.59</td>
</tr>
<tr>
<td></td>
<td>1.20</td>
<td>1.10</td>
<td>1.04</td>
<td>1.00</td>
</tr>
<tr>
<td></td>
<td>Thin PoP Roadmap</td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Integration</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Packaging Trend in Sensors is Going to Fusion!

Sensor | Trim Algorithm | Package | Package Attributes
--- | --- | --- | ---
3-Axis Magnetometer | Data Processing | Non-Ferromagnetic Package | Discrete Sensor Packages
3-Axis Accelerometer | Data Processing | Package
3-Axis Gyro | Data Processing | Package
Pressure Sensor | Data Processing | Cavity Package
Misc: IR, Humidity, Optical, Microphone | Sensor Fusion | Cavity Package
Mag + Accel 6DOF eCompass Sensor | Sensor Fusion | Combo Sensor Package
Accel + Gyro 6DOF Sensor | Reference Mapping & Trim | Fusion Packaging
Mag + Accel + Gyro 9DOF Sensor | Kalman Filter (or similar) | - Multi-Die w/Interconnect
Mag + Accel + Gyro + Pressure 10DOF Sensor | Data Processing | - Low Stress
Misc: IR, Humidity, Optical, Microphone | Cavity Combo Package or Partial Cavity Package | - Cavity or Partial Cavity

Fusion Packaging:
- Multi-Die w/Interconnect
- Low Stress
- Cavity or Partial Cavity
- Multi-Die w/Interconnect
- Very Low Stress
- Solid, Optical or Ported Lid
## MECS / Sensor Products

<table>
<thead>
<tr>
<th>Available</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overmold Laminate cavity</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
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<tr>
<td>Polymer lid cavity</td>
<td><img src="image4.png" alt="Image" /></td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
<tr>
<td>Membrane U-phone</td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
<td><img src="image9.png" alt="Image" /></td>
</tr>
<tr>
<td>Pre-molded (Substrate)</td>
<td><img src="image10.png" alt="Image" /></td>
<td><img src="image11.png" alt="Image" /></td>
<td><img src="image12.png" alt="Image" /></td>
</tr>
<tr>
<td>Exposed sensor</td>
<td><img src="image13.png" alt="Image" /></td>
<td><img src="image14.png" alt="Image" /></td>
<td><img src="image15.png" alt="Image" /></td>
</tr>
<tr>
<td>Pre-molded (Leadframe)</td>
<td><img src="image16.png" alt="Image" /></td>
<td><img src="image17.png" alt="Image" /></td>
<td><img src="image18.png" alt="Image" /></td>
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<tr>
<td>WLCSP MEMS</td>
<td><img src="image19.png" alt="Image" /></td>
<td><img src="image20.png" alt="Image" /></td>
<td><img src="image21.png" alt="Image" /></td>
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<tr>
<td>U phone Pressure</td>
<td><img src="image22.png" alt="Image" /></td>
<td><img src="image23.png" alt="Image" /></td>
<td><img src="image24.png" alt="Image" /></td>
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<tr>
<td>9 axis Inertial Combo</td>
<td><img src="image25.png" alt="Image" /></td>
<td><img src="image26.png" alt="Image" /></td>
<td><img src="image27.png" alt="Image" /></td>
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<tr>
<td>TSV possum sensor</td>
<td><img src="image28.png" alt="Image" /></td>
<td><img src="image29.png" alt="Image" /></td>
<td><img src="image30.png" alt="Image" /></td>
</tr>
</tbody>
</table>
SiP Requirement

Small form factor
- Low profile component (01005/008004)
- 150um Cu pillar

Package size
- 2.0x2.5~25x30 mm

• Possum
• Two side assembly

Conformal shield
- Sputtering

Interconnection
- Flipchip and Wirebond

Embedded passive
# Advanced SiP Design Guideline

<table>
<thead>
<tr>
<th>Item</th>
<th>Production</th>
<th>Development</th>
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</thead>
<tbody>
<tr>
<td>Die to PKG Edge</td>
<td>85</td>
<td>75</td>
</tr>
<tr>
<td>Comp. pad to PKG edge</td>
<td>85</td>
<td>75</td>
</tr>
<tr>
<td>Die to Die</td>
<td>75</td>
<td>65</td>
</tr>
<tr>
<td>Non common net Comp. pad</td>
<td>85</td>
<td>75</td>
</tr>
<tr>
<td>Common net Comp.</td>
<td>60</td>
<td>50</td>
</tr>
<tr>
<td>Metal trace to Comp.</td>
<td>80</td>
<td>70</td>
</tr>
</tbody>
</table>

- Die to die distance 75um
- 01005 Comp. to Comp. distance 85um (Non-common net)
- 0201 Comp. to Comp. distance 85um (Non-common net)
- 01005 Comp. to Comp. distance 60um (Common net)
- 0201 Comp. to Comp. distance 60um (Common net)
- Die to Comp. distance 75um
Amkor’s Experience with Varying End Applications

- **Memory**
  - Same die stack, Pyramid stack, side by side MCM
  - DAF, FOW, Wire Bonding Interconnection

- **Connectivity, Digital, Consumer**
  - WLCSP (FC die) and Wire Bond Stack, Crystal
  - FC+ 2 die stack, die to die bonding, die to PCB bonding
  - MUF (Mold Under Filling)

- **Automotive, Sensor**
  - Sensor Die expose –Film assist molding
  - Double side assembly, Possum FC die
  - TSV, CoC stack
# SiP Technology

<table>
<thead>
<tr>
<th>Available</th>
<th>2015</th>
<th>2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPD (Customer consigned)</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>Core-Less Substrate Pkg</td>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
</tr>
<tr>
<td>Embedded Passive / Die</td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
<tr>
<td>Possum FC</td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
</tr>
<tr>
<td>Two Side assy</td>
<td><img src="image9.png" alt="Image" /></td>
<td><img src="image10.png" alt="Image" /></td>
</tr>
<tr>
<td>Compartment Shield</td>
<td><img src="image11.png" alt="Image" /></td>
<td><img src="image12.png" alt="Image" /></td>
</tr>
<tr>
<td>Conformal Shield</td>
<td><img src="image13.png" alt="Image" /></td>
<td><img src="image14.png" alt="Image" /></td>
</tr>
<tr>
<td>008004 Passive</td>
<td><img src="image15.png" alt="Image" /></td>
<td><img src="image16.png" alt="Image" /></td>
</tr>
<tr>
<td>Double side molding</td>
<td><img src="image17.png" alt="Image" /></td>
<td><img src="image18.png" alt="Image" /></td>
</tr>
<tr>
<td>Recessed Substrate</td>
<td><img src="image19.png" alt="Image" /></td>
<td><img src="image20.png" alt="Image" /></td>
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<tr>
<td>Cavity Substrate</td>
<td><img src="image21.png" alt="Image" /></td>
<td><img src="image22.png" alt="Image" /></td>
</tr>
<tr>
<td>SLIM/SWIFT</td>
<td><img src="image23.png" alt="Image" /></td>
<td><img src="image24.png" alt="Image" /></td>
</tr>
<tr>
<td>TSV</td>
<td><img src="image25.png" alt="Image" /></td>
<td><img src="image26.png" alt="Image" /></td>
</tr>
<tr>
<td>Flex Substrate</td>
<td><img src="image27.png" alt="Image" /></td>
<td><img src="image28.png" alt="Image" /></td>
</tr>
</tbody>
</table>
Si Photonics

- 20um diameter / 40um pitch
- 2~5K bump count (nom)

- Known Good Die
- Both MR & TC available

- Wire bond
- Flip chip (possum)

- Various customized design
- Control for alignment
Technologies for Photonics

Chip on wafer technology

System in Package technology
LAB (Laser Assisted Bonding) Technology for lower stress attach

- **New interconnection solution using laser beam after F/C bonding**
  - Only die heat up with area laser (Local reflow concept)
    - Low thermal stress between PCB and die
  - Fast solder melting: High UPH (Same as mass reflow)

- **Target markets**
  - Mobile, networking, consumer, CPU/GPU
  - BB, AP, logic, ASIC
  - Low K device (28nm, 20nm, 14/16nm)

- **Technology advantage**
  - Cost effective process
  - Lower thermal stress than mass reflow
Amkor MEMS Tester Development

MEMS Technology / Application

- 9DOF (Mag+Accel+Gyro)
- 6DOF (Mag+Accel)
- RF MEMS
- Emerging MEMS
- Optical MEMS
- Temperature
- Humidity
- Pressure
- Gyroscope
- Accelerometer
- uPhone (Top/Bottom)
- E-compass

Development Plan
- Overmolded PKG
- Cavity PKG

Handler conversion

S/W in ATK

H/W in ATP

< 2013

2014

Amkor Developed Solution

2015

Commercial Solution in Amkor production

2016
Global ECO- Society System

Academic Science

Packaging Solution

Material Supply

Design House

Equipment Engineering

Amkor Confidential 33