Virtual Fabrication: Integrated Process Modeling for Advanced Technology

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  • A Virtual Learning Cycle
All the future technology trends point to increased structural complexity
- Cost and development cycle-time will increase
- Systematic structural defectivity becomes the limiter to yield-ramp
- The role of Process Integration becomes essential to development success

Process Integrators need to be armed with the right tools
- Traditional TCAD modeling is useful for individual transistors
- Ab-Initio modeling is useful for novel materials and unit processes
- But the process integrator typically relies on running experimental wafers!
- Trial-and-Error Silicon Engineering is NOT ACCEPTABLE!!!
Integration Modeling

**Equipment Parameters:**
- Process Gas Flows
- RF Plasma Energy
- Chamber Pressure
- CMP Downforce
  etc.

**Behavioral Parameters:**
- **Etch:**
  - Depth
  - Lateral Ratio
  - Selectivity
    (Sputtering Ratio)
    (Plane Dependence)
    (Pattern Dependence)
- **Deposit:**
  - Thickness
  - Conformality
    (Visibility-Limited)
- **CMP:**
  - Stopping
  - Overpolish
    (Dishing Depth)
    (Dishing Lateral Decay)

**Many other processes**

These results can not be combined to produce overall integrated result across designs in a timely manner.
A Powerful 3D Semiconductor Virtual Fabrication Platform

- Applicable to ANY process & ANY layout
- Replaces build & test with **accurate** 3D modeling of large areas & complex process sequences
- Provides validation and visualization of relationships between design and process
- Provides a **predictive** view of design-technology interactions
Voxel Modeling (SEMulator3D)

- Voxel = 3D Pixel
- Created for high performance
  - Medical Imaging, Semiconductor Modeling
- SEMulator3D modeling technology is proprietary, unique and patented
- Unlike other 3D modeling tools, SEMulator3D is very tolerant and does not fail due to small mask or model defects
- Ideal for arbitrarily complex 3D models

Other Process Modeling Tools

- Based on either BREP or moving mesh technology
- Surfaces are modeled with mathematical equations or discrete polygons
- Works for simple, well-defined models
- Fail or become unreliable for very complex topology common in Semiconductor devices

SEMulator3D is more reliable, accurate and faster than any other 3D process modeling tool
Epitaxial growth is sensitive to crystal planes. \(<111>\) directions normally grow slowest and form limiting facets.

<111> facets form due to slow growth on the \(<111>\) planes.

Embedded SiGe in planar technology (Intel, IBM)

22nm Tri-gate (Intel)

FinFET SiGe Epitaxy (with residual oxide)
Physics-driven etch modeling of
- Multi-material film stacks
- Multiple types of etch physics

Key Features
- Etch physics:
  - Redeposition (aka passivation)
  - Sputtering (physical etching)
  - Etch bias (lateral or chemical etching)
Pattern Dependence

- Models account for multiple pattern-dependent effects:
  - Aspect Ratio Dependent Etching (ARDE), RIE Lag, etc.
  - Pattern Density effects: Isolated vs. Nested features
- Works with Basic Etch and MultiEtch process models
- Pattern Dependence feature enabled in Advanced Modeling Package
- Calibration “Wizard” included to make parameter input simple

Large feature etches much deeper, with more lateral bias and higher hardmask consumption.

Features in center of dense array etch deeper than at the edge of the array.

Isolated features etches shallower, with more vertical sidewalls.
Virtual Metrology Operations

- Automate in-line, local measurements of critical technology parameters
- Mimic real in-fab metrology
- Replace slow out-of-fab destructive characterization

**Expeditor** batch processing tool

- Automated, spreadsheet-driven massively parallel parameter studies

Example: DOE study on FinFET Epitaxy on <100> notched wafer: Dependence on pre-epitaxy fin erosion and epitaxial conditions
• Model **CHECKING** requires a more advanced form of measurement

• Structure Search **FINDS** specific criteria, anywhere in the model:
  • Location of minimum spaces, line-widths, thicknesses
  • Number of electrical nets (opens/shorts)
  • Location of minimum material interfaces

48nm Pitch Back End of Line (BEOL) Example

Minimum Insulator  Net ID and Count  V1-M2 Contact  Minimum Cu Width
Meshing Module

(1) SEMulator3D Material View of 64nm BEOL

(2) SEMulator3D Initial Mesh

(3) SEMulator3D Refined Mesh

(4) SEMulator3D Electrical View of M1-V1-M2 Demo Build (5 nets)

(5) CoventorWare View of Imported Volume Mesh

(6) CoventorWare Capacitance Matrix Solution

Meshing allows use of realistic structures for electrical modeling
Continuum of Accuracy

Basic Structural Model: Simplistic depositions and etches, no process details
Perfect for startup integration definition, process visualization, documentation, generated mask verification

Realistic Model: Basic process knowledge, improved geometric accuracy
Perfect for design-technology co-optimization, flow development, testsite structure identification

Calibrated Model: Based on existing HW data
Perfect for IP validation, parasitic extraction, flow optimization

Proprietary Model: Iterative
Perfect for complex predictive problems

Accuracy & Detail – Development Timeframe

4F² BWL DRAM
GAA Si Nanowire
3D NAND Flash
**Obvious:** BEOL processes are pushed to the limit at 14nm

New patterning schemes to achieve density.
New metallization schemes for yield and reliability.

BUT...
1. High aspect ratio integration challenges
2. Variability becoming larger portion of nominal dimensions
3. Parasitic R/C trade-offs driving hierarchical BEOL
4. Next-node BEOL scaling remains non-trivial
Cross-Wafer Uniformity

- Unit process cross-wafer behavior is easily validated from inline metrology
- The cross-wafer requirement is integrated and electrical
  - Costly & time-consuming to verify on HW
- Typical practice involves individual process optimization, driving toward a “flat” profile for all processes
- SEMulator3D provides a predictive methodology for evaluating integrated structural results (using virtual metrology) due to multiple forms of variation across the wafer (using Expeditor)
  - Process Co-optimization
  - Intelligent APC
SEMulator3D models are the intersection of design and process.

Integrated structural response to variations of multiple processes is now impossible to calculate with historical methods due to process complexity.

Different designs respond to process variations differently.

Virtual fabrication enables thorough investigation of design-process interaction.
**Obvious:** FinFET is the transistor architecture for the future of CMOS

Sub-threshold slope from double-gate structure improves power-performance

BUT...
1. 3D structural integration challenges
2. New variability sources: Body thickness/shape, epi, MOL, etc.
3. New parasitic R/C trade-offs
4. Next-node FET scaling remains non-trivial
MOL Variation Analysis

- Predictive process deck built using public TEMs
- Variation analysis using Expeditor batch tool

- Virtual Metrology extracting 3D interface surface area – would require out-of-fab destructive characterization
- Physical parameter serves as electrical sensitivity for resistance or reliability criteria
FEOL Parasitic Extraction

(1) SEMulator3D Material View of FinFET FEOL

(2) SEMulator3D Initial Mesh

(3) SEMulator3D Refined Mesh

(4) SEMulator3D Electrical View of FinFET FEOL Demo Build (4 nets)

(5) CoventorWare View of Imported Volume Mesh

(6) CoventorWare Capacitance Matrix Solution

Meshing allows use of realistic structures for electrical modeling
**Obvious:** Cost/bit NVRAM scaling has introduced *CRAZY* 3D structures

Vertical bit-line integration, multi-layer integration, etc.

**BUT...**
1. High aspect ratio integration challenges
2. Defects in multi-layer stack have wide-ranging implications
3. Further scaling drives more layers... really?!?!?!
**Macro-scale** – Example: Overall Integration

- Large multi-regional structure
- Complex multi-module integration

**Modeling:**

- Large layout area selection
- 1.0 nm resolution
- Basic Etch Model

**Micro-scale** – Example: Plug Etch/Fill

- High aspect ratio etch
- Multi-layer cyclic etch process
- Profile details are critical

**Modeling:**

- Layout area subset
- 0.5 nm resolution
- Advanced Etch Model

**SEMulator3D offers simple flexibility to explore different scales of physical challenges at high speed**
Defect Evolution

60nm metal defect embedded during early phases of multi-layer stack deposition

Defect "magnification" through remainder of stack deposition

Defect blocks "plug etch", kills one bitline (expected). Plug module is robust enough for nearby bitlines to survive, despite non-planarity.

Non-planarity affects "slit etch" later in flow. Results in underetch and shorted control gates. Kills entire sub-array block. NOT EXPECTED!!!

SEMulator3D enables defect evolution understanding for yield ramp calculation and optimization
SEMulator3D in the Market

Cpk Based Variation Reduction: 14nm FinFET Technology

Rohit Pal, Alex Chen, Xing Zhang, Sruthi Muralidharan, Laks Vanamurthy, Girish Bohra, Chloe Yong, Mitsuhiro Togo, Changyong Xiao, Si-Gyung Ahn, Yuan-Hung Liu, Puneet Khanna, Dinesh Koli, Zhe Chen, Owen Hu, Karen Riding, Manfred Eller, Rick Carter, Srikanth Samavedam

22nm Technology Yield Optimization Using Multivariate 3D Virtual Fabrication


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A comparison of the pattern transfer of line-space patterns from graphoepitaxial and chemoepitaxial block co-polymer directed self-assembly

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SEMuulator3D at IMEC

Imec and Coventor Partner Up
by Paul McMillan
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Imec, Coventor partner to advance CMOS process development

**INTERTWINED CHAIN:**
FAILURE DUE TO UNDERSIZED BLK

Target Structure showing independent chains
Target Structure showing SHORTED chains

*Colours = independent electrical loops

OLD design : litho + etch bias
NEW design: litho + etch bias

Undesired epi growth

RMG Fill Process Window

28 nm 15 nm
**Silicon Cycle of Learning:**
- Wafers: 40 WSD * 3 months
  - 150 5-way Experiments
  - All subject to variation
  - All captive to other processes
- Characterization: Additional Resource
- Analysis: Additional Resource
- Cost ~ $50M

**Virtual Cycle of Learning:**
- 150 isolated 5-way Experiments
- 30 minute model build
  - High Resolution (~5A)
- 20 designs: Key Library Elements
- Characterization: Built-in (Virtual Metrology)
- Analysis: Pre-processed (Expeditor)
- 512 CPUs (4 CPUs/case): 2.4 days

Utilize parallel computing infrastructure to dramatically accelerate development!
Conclusion

- Advanced process technologies require Virtual Fabrication
  - Process complexity will impact Logic, SRAM, DRAM, Flash, etc.
- Process development with Virtual Fabrication saves time, money and development resources
- SEMulator3D Virtual Fabrication = more than visualization:
  - Cross-wafer process uniformity optimization and APC
  - Process centering conditions and sensitivity analyses
  - Meshing for electrical analysis such as Parasitic Extraction
  - Process corner analysis and design-process interaction sensitivities
  - Defect evolution exploration and yield-ramp optimization
- Virtual Fabrication benefits all semiconductor user groups:
  - Technology Developers: IDMs and Foundries
  - Fabless: Foundry Interface, IP Validation, DFM
  - Equipment/Process: Process co-optimization, APC, Integration context

Thank you for your time
SEMu1ator3D 5.0

coming soon....