RF SOI: A Deeper Insight for a Faster Time-to-Market
CLIENTS

Wafer producers
Foundries
MEMS fabless
Imaging Industry
RF as a *tool* for the enhancement of many technologies
Bell Labs

1948

22,000,000 /mm²

Microprocessor Transistor Counts 1971-2011 & Moore’s Law

Date of introduction


Transistor count

curve shows transistor count doubling every two years

[wikipedia]
Frank Schwierz
High Resistivity Substrate

SiO₂

System-on-Chip

Processor

RF

WLAN

Base Band

MEMS

PMU

Mixed Signal

Digital

DSP

Memory

Logic CPU/DDR SRAM
GPU/Interface

Power Amp/Power Management

Accelerometer/Gyroscope

RF WiFi/Bluetooth/FM tuner

GSM/3G
Baseband Processor
High Resistivity SOI substrates: how high should we go?

- STD SOI: 20 $\Omega \cdot cm$ ⇒ high losses
- HR SOI of 10 k$\Omega \cdot cm$ would correspond to a lossless Si substrate

Conductor losses ($\alpha_{\text{cond}}$)

Substrate losses ($\alpha_{\text{sub}}$)
Substrate technology

- Compatible with CMOS technology
- Low parasitic conductance/capacitance
- Low RF losses ($\rho > 3 \, \text{k}\Omega\text{-cm}$)
- Low crosstalk
- Linearity ($<-70\text{dBc @ 35 dBm}$)
- High quality passive devices ($\rho > 1 \, \text{k}\Omega\text{-cm}$)
- Availability (mainstream production, size)
- Low cost
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[D. Lederer et al., SOI 2003], [C. Roda Nèves et al., TED’12]
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HR-SOI (as HR-Si) suffers from parasitic substrate effects

[D. Lederer et al., SOI 2003], [C. Roda Neve et al., TED’12]
HR-SOI suffers from Parasitic Surface Conduction (PSC) effect at the SiO$_2$/Si interface.

Parasitic Surface Conduction (PSC)
- Mobile & Interface trapped charges
- Accumulation layer
- Fixed charges
- Highly conductive layer
- n-type

10 kΩ.cm + PSC \(\approx 200 \ \Omega.cm\)

[C. Roda Neve et al., TED’12]
Trap Rich layer freezes the highly conductive layer at BOX – Handle interface
Trap-rich Fabrication

- Proton implantation
  [Wu et al., EDL’00]
- Silicon etching
  [Roda Neve et al., EUMC’07]
- Ar implantation
  [Posada et al., EuMIC’06]
- Oxygen-doped polycrystalline Si
  [Rong et al., EDL’04]
- Amorphous Si
  [Lederer et al., EDL’95]
- Polycrystalline Si
  [Gamble et al., MGWL’99]
- RTA-crystallized Polysilicon
  [Lederer et al., EDL’05]
- Nanocrystalline Si
  [Chen et al., EDL’11]
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trap-rich HR-SOI
RF Non-Destructive Characterization

- **Harmonic Distortion**
- **S-Parameters**
- **Cross Talk**
- **Digital Noise**

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Spreading Resistance Profiling (SRP)

Destructive. Difficult to get detailed wafer mapping.

Does not capture interfacial conduction.

Difficult to relate to final processed RF and Non-linear wafer behavior.

Expensive
Measurement Setup

- **S-parameters & cross-talk** from 5 Hz to 26 GHz
- **THD (H2 & H3)** from -25 to 40 dBm

(900 MHz, 1.8 GHz, 3.6 GHz -> 5 GHz)

HD > -145 dBm (noise floor)

Dynamic range of **165 dBc**
(140 dBc at 40 dBm of input power)
Harmonic Distortions (Large Signal)
Effective Resistivity, Substrate Losses (Small Signal)

Cross Talk through the substrate (Small Signal)

Incize provides its customers with tailored libraries of test structures adapted to their technology for optimized characterization results.
Harmonic Distortions (Large Signal)
Effective Resistivity, Substrate Losses (Small Signal)

Incize is developing the first *defacto* Standard for substrate characterization.

Harmonized FoM Optimized Geometries Enhanced Efficiency
trap-rich HR-Si
HR-Si

Lossless linear reference
Quartz

$\rho_{\text{Si}} \rightarrow$ from 10 $\Omega$ to 10 k$\Omega$-cm

t$_{\text{ox}} \rightarrow$ from 50 to 1000 nm

48 substrates
Small Signal Characterization

<table>
<thead>
<tr>
<th></th>
<th>$\rho_{\text{nom}}$ [(\Omega)-cm]</th>
<th>$\rho_{\text{eff}}$ [(\Omega)-cm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>std-Si</td>
<td>10</td>
<td>33</td>
</tr>
<tr>
<td>HR-Si</td>
<td>(&gt; 5\ k)</td>
<td>64</td>
</tr>
<tr>
<td>Quartz</td>
<td>-</td>
<td>(&gt; 5\ k)</td>
</tr>
<tr>
<td>trap-rich HR-Si</td>
<td>(&gt; 5\ k)</td>
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</table>

Error in $\rho_{\text{eff}}$ extraction due to VNA accuracy (freq. dependent)

$Q_f \sim 3 \times 10^{11}$

[Roda Neve et al., EUMIC’08]
TR HR-SOI substrate meets harmonic distortion switches specifications.

[K. Ben Ali, SiRF 2014]
Large Signal Characterization

CPW 2146 µm-long

Graphs showing the relationship between bias voltage ($V_{\text{bias}}$) and harmonic distortion ($HD_2$, $HD_3$) for different materials:
- StdSOI
- HR-SOI
- TR-SOI
- Quartz

The graphs display the following ranges:
- $V_{\text{bias}}$: -100 to 100 V
- $HD_2$ (dBm): -20 to 0 dBm
- $HD_3$ (dBm): -120 to -60 dBm
Crosstalk on HR and TR-SOI

 teste structure

150 x 50 µm²

\(d = 50\ µm\)

HR-SOI
TR-SOI
SOS

[K. Ben Ali et al., TED’11]
Crosstalk on HR and TR-SOI

Test structure

<table>
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<th>S21 [dB]</th>
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<td>150 x 50 µm</td>
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<tr>
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[K. Ben Ali et al., TED’11]
Digital Substrate Noise

- **Noise Source (digital)**
- **Victim (analog)**

**Substrate Coupling**

- Bulk Si / SOI HR-Si

**UCL’s SOI FD MOSFET**

- NP2N
  - $L = 2 \mu m$
  - $W = 20 \mu m$
  - $N_f = 20$

**RF in**

- 900 MHz

**Mixed Output**

- 900 MHz

**Noise**

**Limited DSN reduction due to PSC**

[D. Bol et al., SOI'07]
Digital Substrate Noise

Without Noise

Noise: square signal @ 500 kHz

Almost 25 dB reduction of the coupled noise.

TR-SOI reduces Digital Substrate Noise

[Ref. 2012]
Inductors on TR HR-SOI wafer show
• Improved Q
• Reduced substrate harmonic distortions

Integrated Inductors on TR-SOI

Measured results of 35 μm-thick 2 nH spiral inductors on HR-Si and Trap-Rich HR-Si

[K. Ben Ali, SiRF 2014]
Impact of neutron irradiation

- Displacement Damage + secondary ionizing effects ($h^+\text{-}e^-$ pairs)
- Induced fixed charges
- Induced interface traps
- Doping variation & Carrier mobility degradation

[C. Roda Neve, RADECS 2009]
Impact of neutron irradiation

- Fast neutron beam
- High neutron flux and mean energy of 20 MeV
- Ambient temperature
- Neutron fluence up to $2.2 \times 10^{14}$ neutrons/cm$^2$
- Passive regime → devices are not biased

![Graph showing frequency vs. attenuation before and after irradiation for different thicknesses of SiO$_2$ with and without PSi.]

- Loss reduction after irradiation (no PSi):
  - 0.4 dB/mm $\rightarrow$ 50 nm
  - 0.5 dB/mm $\rightarrow$ 500 nm

- Final attenuation after irradiation (no PSI):
  - $\alpha_{500 \text{ nm}} > \alpha_{50 \text{ nm}}$

- Almost no variation for substrates with PSi

[C. Roda Neve, RADECS 2009]
Impact of TR-SOI on Active Devices

Academic process
UCL SOI CMOS technology

FD SOI MOSFETs  400 nm BOX
80 nm SOI
25 nm gate oxide

Gate Length (L):  2 µm
# fingers: 20
Finger width (W): 20 µm
Chanel doping: NP2N - Boron implantation
(4 x 10^{16} at/cm^3)

[K. Ben Ali, SOI Conf. 2012]
Impact of TR-SOI on Active Devices

TR HR-SOI shows no impact on Active Devices performance

Commercial PD SOI MOSFET
Foundry technology 5-metal layers, $L_g < 0.3 \, \mu m$

[K. Ben Ali, SOI Conf. 2014]
<table>
<thead>
<tr>
<th>Feature</th>
<th>SOI</th>
<th>HR-SOI</th>
<th>SOS SOQ</th>
<th>Trap-rich HR-SOI</th>
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<td>Low crosstalk ((f &lt; 10 \text{ GHz}))</td>
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<td>✔</td>
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<tr>
<td>Availability (mainstream production, wafer size)</td>
<td>✔</td>
<td>✔</td>
<td>?</td>
<td>✔</td>
</tr>
<tr>
<td>Low cost</td>
<td>✔</td>
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<td>✗</td>
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**TR-SOI substrate is the most promising solution for RF SoC, and future LTE, 5G generations.**
**Take Away**

**RF** is not only for high frequency operation, it is a powerful **tool** to enable many technologies.

*Incize* is developing the first **standard** to optimize the substrate characterization.

**Trap-Rich HR** SOI is THE technology for next generations of **HF** applications.
Acknowledgments

**Incize Team:** Dr. Khaled Ben Ali and Dr. Sergej Makovejev

**UCL:** Prof. Jean-Pierre Raskin and his group. Winfab and WELCOME teams.

Dr. Cesar Roda Neve from IMEC (ex-UCL).
thank you!