FDSOI TECHNOLOGY:
GENERAL OVERVIEW & LOW-POWER DESIGN

SITRI FDSOI workshop I 08/09/2016
OUTLINE

- FDSOI technology overview
  - From bulk to UTBB-FDSOI
  - FDSOI technology flavors
  - Comparison between the different options

- UWVR & ULV applications
  - FRISBEE UWVR test chip & design techniques
  - UWVR memory
  - ULV memory
  - ULV design gain
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  • ULV memory
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SOI ARCHITECTURES LANDSCAPE

- **Fully Depleted SOI**
- **Partially Depleted SOI**
- **Extremely Thin SOI**
- **Ultra thin Body & Box**

**Bulk Planar**
- Low Electrostatic performance
- Low VT modulation capability

**PD-SOI**
- Low Electrostatic performance
- Low VT modulation capability

**ET-SOI**
- Good Electrostatic performance
- Low VT modulation capability

**UTBB**
- Good Electrostatic performance
- Efficient VT modulation capability

**Extremely Thin SOI**
- **Front Gate**

**Ultra thin Body & Box**
- **Back Gate**
CMOS UTBB-FDSOI DEVICES

1- Gate stack
High k ($C_{\text{OX}}$)
Metal-Gate
($V_T$)

2- Raised SD (RSD $\downarrow$)

3- Si-film ($\approx L_g/3$)
No channel doping
No pocket implant

4- BOX (25 nm)

5- Back plane or WELL ($V_T$)

6- Back Biasing

7- Isolation (STI)
28FDSoI & BODY BIAS (BB) FLAVORS

**Regular Well (RW) – Reverse BB**
- NMOS
- PMOS
- Vddsp
- Gndsn
- p-Well
- n-Well

**Flip Well (FW) – Forward BB**
- NMOS
- PMOS
- Gndsp
- Gndsn
- n-Well
- p-Well

**Vth↑ & Idq↓**
- RBB
- FBB

-3V (-1.8V)  
Vdd/2+ 300mV

-300mV

+3V (+1.8V)

Vth↓ & Idq↑
SINGLE-WELL OPTION

FBB & SNW co-integration

FBB

SNW

RBB & SPW co-integration

A. Valentian et al., S3S 2015
FBB/RBB/SN(P)W RELATIVE PERFORMANCES

[A. Valentian et al., S3S 2015]
UTBB FDSOI AND ENERGY EFFICIENCY

![Energy Consumption Graph](image)

- **Blue**: $E_{\text{Total}}$
- **Red**: $E_{\text{Dyn}}$
- **Green**: $E_{\text{Stat}}$

- $V_{BB} \{2, -2\}$
- LVT
- ZBB
- RVT
- $V_{BB} \{-2, 2\}$

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RVT FDSOI-based Full Adders present less energy consumption, although the slowest behavior.

Bulk ones show the worst overall performance.

VBB knob allows FDSOI performance adaptation.

Better variability allows a lower Vdd operation.
CONCLUSION: A NEW LANDSCAPE FOR DESIGNERS

• FDSOI is a new landscape for designers, opening different optimization choices:
  • RBB / FBB islands choices
  • Poly-biasing / single well options
  • Dynamic control of FBB/RBB

• But also:
  • New IP designs
  • Better process variability control
  • RF/analogue with best-in-class characteristics
Regular Well (RW) – Reverse BB

Ultra-Low leakage
=> always-on, low performance

Flip Well (FW) – Forward BB

Energy efficiency
=> Continuum of performance (UWVR)
=> performance @ Low voltage
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  • FRISBEE UWVR test chip & design techniques
  • UWVR memory
  • ULV memory
  • ULV design gain
# AN OVERVIEW OF FDSOI DIGITAL CIRCUITS @ LETI

<table>
<thead>
<tr>
<th></th>
<th>FRISBEE</th>
<th>SRAM Defect</th>
<th>VIDOCQ</th>
<th>DIPMEM</th>
<th>SHARP</th>
<th>RUSH (LIOT)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
<td>FDSOI 28nm</td>
<td>FDSOI 28nm</td>
<td>FDSOI 28nm</td>
<td>FDSOI 28nm +</td>
<td>FDSOI 28nm</td>
<td>FDSOI 28nm</td>
</tr>
<tr>
<td><strong>Main features</strong></td>
<td>Ultra Wide Voltage Range DSP</td>
<td>Characterization of FDSOI Memory</td>
<td>Ultra Wide Voltage Range Memory</td>
<td>Mixing SRAM and NVM for fast switch-on/off.</td>
<td>Low-power multicore</td>
<td>ULV design for always-on devices</td>
</tr>
<tr>
<td><strong>Architecture</strong></td>
<td>32-bit VLIW Serial interface Wide range FBB</td>
<td>1K x 32bits memory with embedded BIST</td>
<td>1K x 32 bits memory</td>
<td>Multi-banks architecture</td>
<td>MIPS based multicore with L1, L2, L3 mem.</td>
<td>ARM M0+ core + peripherals</td>
</tr>
<tr>
<td><strong>Design</strong></td>
<td>UWVR SRAM and libraries Timing monitoring Pulsed latch FF</td>
<td>Embedded full characterization scheme. 6T SRAM cell, high density</td>
<td>8T SRAM cells. Write-assist scheme. Mixed-well logic design.</td>
<td>Mixed SRAM/NVM with common periphery. Context saving</td>
<td>3D Chiplet using 3D plugs Network-on-Chip Cache-coherency</td>
<td>0,5V design ULV memory</td>
</tr>
<tr>
<td><strong>Main Results</strong></td>
<td><a href="mailto:2.6GHz@1.3V">2.6GHz@1.3V</a> 460MHz@397 mV 370mW@1V 62pJ/cy@0.46V</td>
<td>Full charac. of RA, WA, WS with pulse width between 350ps and 30ns</td>
<td>400 mV min. Voltage 1,5Ghz @ 1 V</td>
<td>On/off in less than 1 µs. Zero leakage architecture when off.</td>
<td>800 Mhz MIPS Scalability demonstrated with 96 cores integration.</td>
<td>50 MHz @ 0,5V</td>
</tr>
</tbody>
</table>
**Objectives:**
- Ultra-Wide Voltage Range (UWVR) operation: \( V_{dd} = [0.3\text{V}-1.3\text{V}] \)
- High performance
  - \( F_{cl} > 2.7\text{GHz} @ 1.3\text{V} \) - \( F_{cl} > 200\text{MHz} @ 0.35\text{V} \)
- Power-efficiency

**Frisbee Characteristics:**
- 32-bit data-path VLIW DSP (FFT 1024)
- UWVR 8T SRAM cuts (1Kx32) with read/write assist
- FBB/RBB IOs delivering from -2V to 2V
- UWVR standard cells (with 2 different poly-bias)
- Pulsed latches for high performance FF
- Timing margin reduction mechanism implemented (fault detectors, replica paths, fine-grain clock generator)

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**FRISBEE: A PROTOTYPE FOR DEMONSTRATING FDSOI**

- FDSOI 28nm FlipWell
- Area = 1 mm²
- Gate nb = 2 Millions
FDSOI APPLIED TO AN UWVR DSP

[Beigne et al. JSSC 2015]
FDSOI BENEFICE FOR ASYMMETRIC GATES

- Asymmetric PB in library cells allows UWVR optimization
- New FF designs regain interest: Pulsed-latch

![Diagram of FDSOI BENEFICE FOR ASYMMETRIC GATES](image)

<table>
<thead>
<tr>
<th>Design</th>
<th>D-to-Q (ps)</th>
<th>Egy/cycle (fJ)</th>
<th>Area (μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST C2MOS</td>
<td>117.5</td>
<td>6</td>
<td>4,41</td>
</tr>
<tr>
<td>ST SA</td>
<td>46.5 (- 60 %)</td>
<td>12.5 (+ 208 %)</td>
<td>6,85 (+ 55 %)</td>
</tr>
<tr>
<td>TGPLMuxScan</td>
<td>30.5 (- 74 %)</td>
<td>7.2 (+ 20 %)</td>
<td>4,73 (+ 7 %)</td>
</tr>
<tr>
<td>TGPLMuxClk</td>
<td>26 (- 78 %)</td>
<td>9.1 (+ 56 %)</td>
<td>5,06 (+ 14 %)</td>
</tr>
</tbody>
</table>
FDSOI allows running at large voltage range
- FDSOI has reduced variability compared to bulk
  - Larger energy or performance gains promises
- LETI has developed a full methodology for getting benefits or this advantage with dedicated IPs

VARIABILITY / POWER CONTROL IN FDSOI : ADVANTAGES
• Estimate and track the Fmax on Wide Voltage Range
• Generate statistics in order to minimize the detection margin
• Avoid pushing the IP to timing failure
  • Avoid recover-after-error mechanism (Razor)
• Reduced number of sensors (low area overhead)
• Without test-time overhead
• The characterization done in-situ (final product)
• Re-characterize periodically the circuit to compensate the ageing
TMFLT METHODOLOGY

Calibration

Functional test

TMFLT-Sensors

Margin reduction

Fmax estimation

Calibration

Voltage

Frequency

TMFLT-Ring

Periodic recharacterization for ageing

CEA patent

Run-time

IR drops

TMFLT-Ring

Frequency instability

Warning
• Similar approach to Canary Flip-Flop
• It uses a large detection window
  • Anticipate the error detection instead of just detect the error
  • Therefore, a non-critical path can be used to anticipate the errors
• No need to instrument the most critical paths of the circuit
• Reduced number of sensors
• Low area footprint = equivalent to 2 FF, integrated as standard cells
• Negligible performance impact
Based on a time-to-digital converter, it measures the propagation time through a programmable delay element and compares it with the clock period.

- One measure every two clock cycles
- 300 µm² in FDSOI 28nm
• Measures on a 28nm FDSOI circuit (Frisbee)
• Nominal clock frequency 1.6GHz at 1V
• Using 21 dies on 3 wafers
• Only 10 TMFLT sensors were used
• Estimation error between the real and the estimated Fmax of the circuit:

Beigne, E. et al., “A 460 MHz at 397 mV, 2.6 GHz at 1.3 V, 32 bits VLIW DSP Embedding F MAX Tracking,”
VARIABILITY / POWER CONTROL IN FDSOI: RESULTS

30mV IR-drop margin

VDD margin (mV)

Frequency (MHz)
FDSoI DESIGN: F/VDD/VBB CHOICES

[Beigne et al. JSSC 2015]
High Energy Efficiency can be obtained @ good performance

[Beigne et al. JSSC 2015]
FDSoI POSITIONING WRT STATE-OF-THE-ART

[Beigne et al. JSSC 2015]

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Technological gains (compared to Bulk):
- Frequency: +90% @ Vdd=1V, +800% @ Vdd=0.5V
- Energy: -60% @ same frequency

Circuit techniques gains:
- 8T SRAM (@ Vdd=0.3V):
  - Write margin (µ/σ): 8.75 (instead of 1.1)
  - SNM (µ/σ): 5 (instead of 1.2)
- Pulsed-Latch:
  - 3x faster than conventional Master-Slave Flip-Flop

Methodology gains
- Reduction of timing margins:
  - Frequency gain up to 25%, energy gain up to 45% (compared to WC design methodology)
Objectives:
- Characterize SRAM cut perf.
- Characterize SRAM bit cell perf.
- Track small defects (RTN, Aging)
- Extract yield vs. VDD & FREQ

Design:
- ST 28nm 5U1x 2T8x LB
- 65kb SRAM (x2) + BIST + PG
- 0.120μm² HDLL 6T SRAM cell
- Pulse width: 350ps up to 30ns

Static and Dynamic characterization
Photograph

**BER vs $V_{DD}$**

- $V_{PW} = 0V$
- Graph showing BER vs VDD with points for RS, RA, and WA.

**SRAM failure map**

- Graph showing failure map with columns and rows indicating failure points.

**Failure mechanisms**

- $V_{MIN}$
- Graph showing $V_{MIN}$ vs WL pulse width (nS) with points for RA, RS, and WA.

**Static consumption**

- Graph showing static consumption vs VDD with a peak at $13.7\text{pA}$.

**ESSDERC’14, IEDM’14**
- Typically weak point in power management techniques
  - Vidocq chip
- FDSOI 28nm
- Energy per access (32b) \( \approx 2pJ @1V \) (Etat de l’art: 3pJ)
- Performance >1.5GHz @1V
- \( V_{\text{min}} \approx 400mV \)
UWVR 32KB SRAM CUT

SPW-NW 8T bit-cell

Mixed-SW Row Decoder

SOI-Conference’13, SOI-Conference’14, DAC’14
UWVR 32KB SRAM CUT: IMPROVED VARIABILITY

SOI-Conference’13, SOI-Conference’14, DAC’14
UWVR 32KB SRAM CUT: RESULTS

SOI-Conference’13, SOI-Conference’14, DAC’14
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ULTRA-LOW-VOLTAGE MEMORY DESIGN

• **Constraints:**
  - Vdd = 0.5V
  - Fmax = 32 Mhz

• **Optimizations:**
  - Single-Pwell memory matrix
  - Single-Nwell periphery
  - Hierarchical power-gating of buffers
  - Multi Poly-Bias optimization

• **Results**
  - Area = 0.02 mm²
  - P_\text{leak} = 1.97 \mu W @ \text{ff} 55°C
  - P_{\text{dyn}} = 1.37 \mu W/\text{MHz} @ \text{ff} 55°C
ULV DESIGN: FDSOI BOOST

- DSP + SRAM @ Iso-Performance (32 MHz)
SUMMARY

• FDSOI allows Ultra-Wide-Voltage-Range thanks to dynamic VT control
• Burst modes COMBINED with high energy efficiency point is now affordable
• ULV design optimization can provide up to 80% gains wrt bulk

⇒ LETI added value is to share his knowledge and methodology, to provide the IPs and the control algorithms for statically and dynamically managing the performance / energy efficiency / low leakage tradeoffs