• 3 back-end options available

• Routing possible on the AluCap level \( \Rightarrow \) no restriction vs. 0.7% in 65 nm
**UTBB 28 nm FD-SOI : RF DIRECT BENEFITS (2/2)**

- **Capacitors**

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Density (Typical)</th>
<th>Observation</th>
</tr>
</thead>
<tbody>
<tr>
<td>egncap</td>
<td>10.1fF / µm²</td>
<td>GO2 device (thick gate oxide)</td>
</tr>
<tr>
<td>CMOM - M1 to M5 (max)</td>
<td>6.45fF / µm²</td>
<td>Space(finger) = Width(finger) between 50 and 100 nm Vmax = 1.1V for S=W &lt; 80 nm Vmax = 1.8V for S=W &gt; 80 nm</td>
</tr>
<tr>
<td>CMIM</td>
<td>16.2fF / µm²</td>
<td>process option: add 3 masks Total area max = 24.6mm² Vmax = 1.155V</td>
</tr>
<tr>
<td>Ivtntfet (Vg=1V ... Vx=0V)</td>
<td>~18fF / µm²</td>
<td>Used as loop filter or supply bypass capacitor Depends on the config. Low capacitance for low voltage.</td>
</tr>
<tr>
<td>Ivtptfet (Vb=1V ... Vx=0V)</td>
<td>~17fF / µm²</td>
<td>Used as loop filter or supply bypass capacitor Depends on the config. Low capacitance for low voltage.</td>
</tr>
</tbody>
</table>

- Very good density / less parasitics to substrate
- Interesting MIM capacitor quality factor
- All required devices for RF exist in FD-SOI
ACTIVE DEVICES PERFORMANCE AND COMPARISON

- No channel doping: better gain compared to bulk
  - At 0.18 µm gate length, the analog gain Gm/Gd in weak inversion in FD-SOI 28nm is higher than the 180 nm CMOS

<table>
<thead>
<tr>
<th></th>
<th>0.18CMOS</th>
<th>28nmBulk</th>
<th>FDSOI28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gm/Gd</td>
<td>50</td>
<td>25</td>
<td>75</td>
</tr>
</tbody>
</table>

- At 1 µm gate length, the Gm/Gd on FDSOI is 6 times larger than the CMOS 28 nm bulk

<table>
<thead>
<tr>
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<th>FDSOI28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gm/Gd</td>
<td>50</td>
<td>300</td>
</tr>
</tbody>
</table>
UTBB-FDSOI 28nm FOR ULP RF (2/4)

HIGH SPEED ANALOG PERFORMANCE

- Lower Vth, less variability
  - Design at Low Power supply
  - High dynamic range
    - With respect to $V_{DD}$ versus $V_{th}$
    - Analog compatible minimum gate lengths

- Reduced S/D capacitances
  - Increased comparator BW
  - Faster logic
  - Reduced switch parasitic
  - Less Power consumption
HIGH RF PERFORMANCES ON BOTH FRONT- & BACK-GATE

• Front Gate FT: faster transistor even at low power supply
  • FT: 300 GHz @ 1 volts $V_{DD}$
  • FT: 150 GHz @ 0.3 Volts $V_{DD}$

• Back gate useful for RF $\Rightarrow$ simple design
  • FT: 80 GHz @ 1 volts $V_{DD}$
  • FT: 40 GHz @ 0.3 volts $V_{DD}$

MEASUREMENTS DONE at LETI
LOW NOISE PERFORMANCE

- $\text{NF}_{\text{min}} \approx 0.2\text{dB} \ (F = 2 \text{ GHz}), \approx 0.4\text{dB} \ (F = 10 \text{ GHz})$
- Noise performances similar to 28nm Bulk

$\text{Ids}=135 \text{ mA/mm, Lg}=30\text{nm}$

[1] Y. Tagro et al "RF Noise Investigation in High-k/Metal Gate 28-nm CMOS Transistors" IEEE IMS, June 2012
UTBB-FDSOI 28nm: FROM RF TO mmW

- Active devices performance and comparison (RF)
  - Higher Gain than CMOS 28 nm & 65nm technology

4 dB gain improvement with respect to CMOS 65nm at 2.4GHz
UTBB-FDSOI 28 nm FOR ULTRA LOW POWER RF

- **Passive devices performance**
  - Typically, the CMOS trend to vertically shrink of the Back-End Of Line (BEOL) penalizes RF performances
  - The small metal pitch and the thin dielectrics increase the Resistance/Capacitance ratio

1.5nH inductor offers 25 Q factor value in UTBB-FDSOI 28nm
CMOS 65 nm vs FDSOI 28nm: RF BENCHMARK

• Comparison between two usual RF blocs
  • LNA and VCO

• Technology use:
  • CMOS 65 nm: 7 metal layers from STMicroelectronics
  • UTBB-FDSOI 28 nm: 10 metal layers from STMicroelectronics

• Transistor models
  • PSP or BSIM for CMOS 65nm
  • UTSOI 2 for UTBB-FDSOI 28nm

90nm BLE/15.4/15.6 Transceiver
LOW NOISE AMPLIFIER : 2.4GHZ TEST CIRCUIT

- Degenerated cascade topology
- $L_s$ and $L_g$ inductance used to match noise and input impedance (target $<-10\text{dB S11}$)
- Gain is evaluated considering $Z_{out} = \text{LNA conjugate output impedance}$
- Same inductor Q value (ideal component with set Q factor)

<table>
<thead>
<tr>
<th></th>
<th>CMOS 65nm</th>
<th>UTBB-FDSOI 28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS Family</td>
<td>N-lvt</td>
<td>N-lvt</td>
</tr>
<tr>
<td>Inductance Q value</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Nominal Vdd (V)</td>
<td>1.2</td>
<td>1</td>
</tr>
</tbody>
</table>
CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

LOW NOISE AMPLIFIER : 1 mW SCENARIO

<table>
<thead>
<tr>
<th>FoM</th>
<th>CMOS 65nm</th>
<th>UTBB-FDSOI 28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>NFmin (dB)</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>Gain* (dB)</td>
<td>21</td>
<td>25</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-11</td>
<td>-16</td>
</tr>
<tr>
<td>PDC (mW)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-15</td>
<td>-15</td>
</tr>
<tr>
<td>ICP1 (dBm)</td>
<td>-24</td>
<td>-24</td>
</tr>
</tbody>
</table>

*Power Gain considering a perfect match output

4dB gain improvement in FD-SOI for same power

LETI BENCHMARK 2015
CMOS 65 nm vs FDSOI 28nm: RF BENCHMARK

LOW NOISE AMPLIFIER: ULTRA LOW-POWER SCENARIO

<table>
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<tr>
<th>FoM</th>
<th>CMOS 65nm</th>
<th>UTBB-FDSOI 28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>NFmin (dB)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>21</td>
<td>24</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-10</td>
<td>-10</td>
</tr>
<tr>
<td>$P_{DC}$ (mW)</td>
<td><a href="mailto:0.4@1.2V">0.4@1.2V</a></td>
<td><a href="mailto:0.1@0.55V">0.1@0.55V</a>*</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-30</td>
<td>-26</td>
</tr>
<tr>
<td>ICP1 (dBm)</td>
<td>-39</td>
<td>-36</td>
</tr>
</tbody>
</table>

*Using body bias = 350mV

X4 power consumption decrease with same RF performances

LETI BENCHMARK 2015
CMOS 65 nm vs FDSOI 28nm : RF BENCHMARK

TEST CIRCUIT : 2.4GHz

- **VCO**

- CMOS cross-coupled topology
- Same inductor Q value
  - Ideal component with set Q factor

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<tr>
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<th>CMOS 65nm</th>
<th>UTBB-FDSOI 28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS Family</td>
<td>N-lvt / P-lvt</td>
<td>N-lvt / P-lvt</td>
</tr>
<tr>
<td>Tank Q value</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Nominal Vdd (V)</td>
<td>1.2</td>
<td>1</td>
</tr>
</tbody>
</table>

LETI BENCHMARK 2015
### CMOS 65 nm vs FDSOI 28nm: RF Benchmark

**VCO: 1 mW / 0.2 mW Scenario**

<table>
<thead>
<tr>
<th>FoM</th>
<th>CMOS 65nm</th>
<th>UTBB-FDSOI 28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (GHz)</td>
<td>2.4</td>
<td>2.4</td>
</tr>
<tr>
<td>Phase Noise (1MHz in dBc/Hz)</td>
<td>-119</td>
<td>-126</td>
</tr>
<tr>
<td>$P_{DC}$ (mW)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Phase Noise (1MHz in dBc/Hz)</td>
<td>-105</td>
<td>-117</td>
</tr>
<tr>
<td>$P_{DC}$ (mW)</td>
<td>0.2 @ 0.8V</td>
<td>0.2 @ 0.7V</td>
</tr>
</tbody>
</table>

**LETI Benchmark 2015**

7 dB to 12 dB Phase Noise improvement for the same power consumption

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SPECIFIC FDSOI BENEFITS FOR LNA

- Evaluation of the performance
  - For the Gain in V (dB)
  - For the NF (dB)

- Making use of the Back-Gate
BACK-GATE CONTROL FOR LNA (1/3)

Bulk: $V_{bg} = V_{dd}$

Various case considering $V_{bg} \neq V_{dd}$

FDSOI: good candidate for ULV use

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BACK-GATE CONTROL FOR LNA (2/3)

FDSOI: good candidate for reconfigurability
BACK-GATE CONTROL FOR LNA (3/3)

\[ FOM = \frac{Av.\ freq.\ IIP3}{(F_{\text{min}} - 1)(I_d \cdot V_{dd})} \]

FoM | ITRS

- BG Variations → Vdd Reduction → FoM improvement

| Vdd | 1,2 | 1 | 0,8 | 0,6 |

Bulk

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ULP RF – ALWAYS ON / WAKE-UP REALIZATION

- **Multi band capability**
  - 868-915 MHz / 1.4 GHz / 2.4 GHz
  - Highly Flexible: Carrier Frequency, Modulation, Channel condition, etc...
  - No costly external component
  - Improved Robustness

- **Adaptive power consumption**
  - Event-driven activity
  - Target to burn \(~50\ \mu W\) in active mode
  - Analog front-end to demodulation: 20 \mu W
  - Synthesizer and LO: 30 \mu W

- **Fast power-on time**

- **Low-cost and easy implementation**
  - Inductorless design
  - Calibrationless design
  - FD-SOI 28 nm

Snapshot of the full Wake-Up RX

LETI FULL FRONT-END 2016

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HIGH-SPEED MODULATOR DRIVER - BULK

- **CMOS bulk**
  - Additional circuitry required
  - Keep cascoded transistors in the Safe Operating Area

- **Avoid $V_{ds} > 1.2\, V$**

![Circuit Diagram]
• **FDSOI 28 nm**
  - Back-Gate allows Vth reduction ➔ no Vds over-voltage
  - Very High Speed communications: 25 Gbps

![Circuit Diagram](image-url)
WIRELESS COMMUNICATION: FD-SOI VS BULK

- Gain improvement (no channel doping)
- Higher speed / analog performance / reduced parasitics
- Higher Passive Quality factors (Metal options & reduced S/D cap.)
- Lower power and higher dynamic range / Lower $V_{TH}$
- Higher frequency operation / faster transistors for lower power
- Easier design / Back Gate as a Static & Dynamic

<table>
<thead>
<tr>
<th>1μm Length</th>
<th>28nm Bulk</th>
<th>FD-SOI 28nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gm/Gd</td>
<td>50</td>
<td>300</td>
</tr>
</tbody>
</table>

Better Gain
Better Phase Noise
Ultra Low Power

FD-SOI RF Design
CURRENT OFFER FROM LETI in FD-SOI

- ULP RF Front-End : TX and RX
- ULP Always-On RX Front-End
  - Wake-up function / spectrum sensing (2015 / 2016)
- Very High Speed Optical Driver / Modulator / Receiver
  - Increase speed rate to tackle the 56 Gbps (2016)
- Fast & High-Resolution ADC : 100 MSpsp / 12 bits
  - General purpose / Low Power for RF Front-End (2016 / 2017)